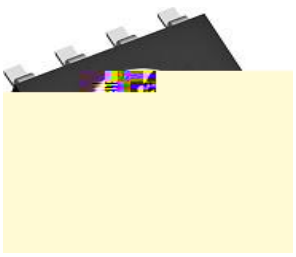
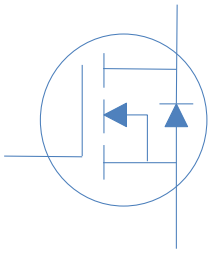
70V N-Ch Power MOSFET

V_{DS}		70	V
$R_{DS(on),typ}$	V_{GS}=10V	7	m
$R_{DS(on),typ}$	V_{GS}=4.5V	10	m
$I_{D\ (Sillicon\ Limited)}$		14	A





Part Number	Package	Marking
HGS085NE6AL	SOIC-8	GS085NE6AL

Absolute Maximum Ratings at T_j

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C	14	A
		T_C	9	
Drain to Source Voltage	V_{DS}	-	70	V
Gate to Source Voltage	V_{GS}	-	20	V
Pulsed Drain Current	I_{DM}	-	56	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.4mH, T_C	45	mJ
Power Dissipation	P_D	T_C	3	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Lead	R_{JL}	25	
	R_{JA}	40	
Thermal Resistance Junction-Ambient (steady state)		75	

Electrical Characteristics at T_j

Static Characteristics

Parameter					max	
Gate Threshold Voltage				1.6	-	
Gate to Source Leakage Current	I_{GSS}	V_{GS} $_{DS}$=0V	-	-	100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=10A		7	8.5	m
	$R_{DS(on)}$	V_{GS}=4.5V, I_D=5A	-	10	13	m
				29	-	S
Gate Resistance	R_G			1.4	-	
			-	1170		
			-		-	pF
			-	31	-	
Total Gate Charge						
Total Gate Charge	Q_g(4.5V)					nC
Gate to Drain (Miller) Charge	Q_{gd}					
Turn on Delay Time	$t_{d(on)}$					
		V_{DD}=30V, I_D=10A, V_{GS}=10V, R_G=10 ,				ns
Fall Time	t_f		-	5	-	

Fig 1. Typical Output Characteristics

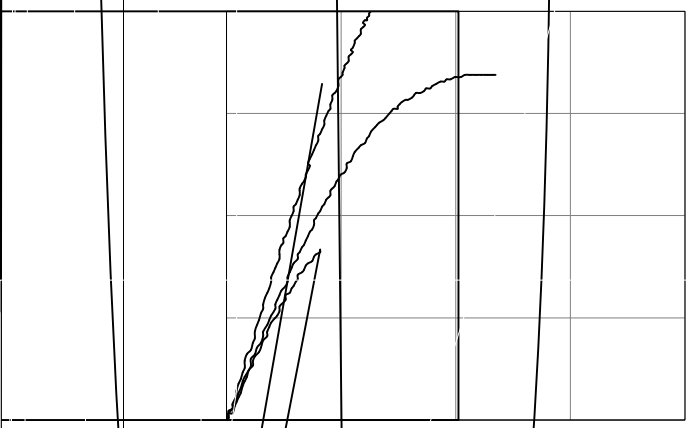


Figure 2. On-Resistance vs. Gate-Source Voltage

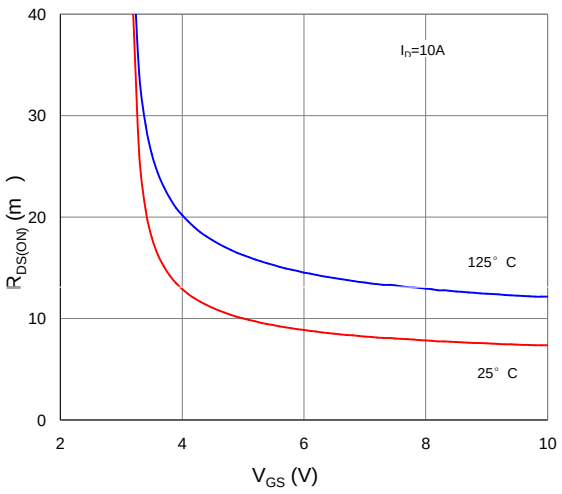


Figure 3. On-Resistance vs. Drain Current and Gate Voltage

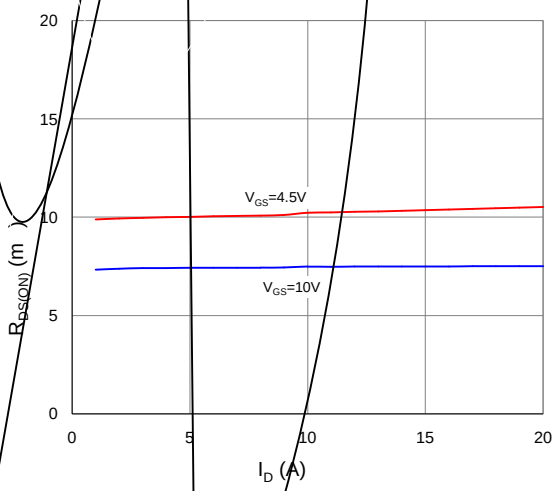


Figure 4. Normalized On-Resistance vs. Junction Temperature

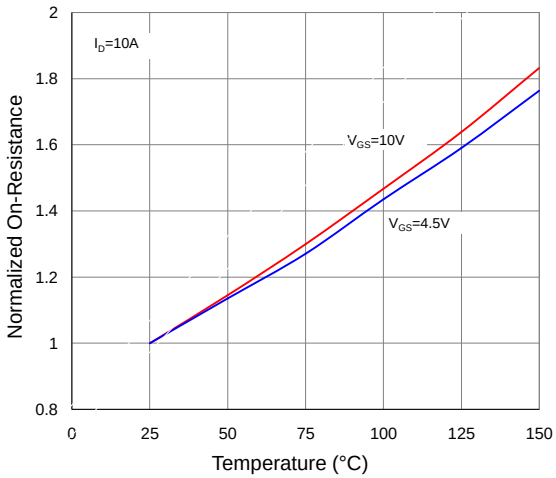


Figure 5. Typical Transfer Characteristics

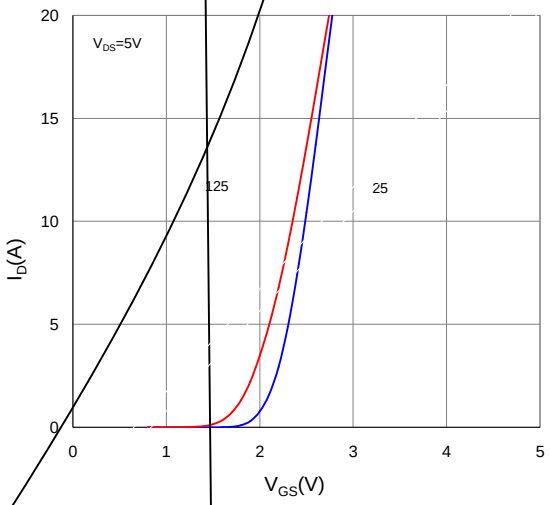


Figure 6. Typical Source-Drain Diode Forward Voltage

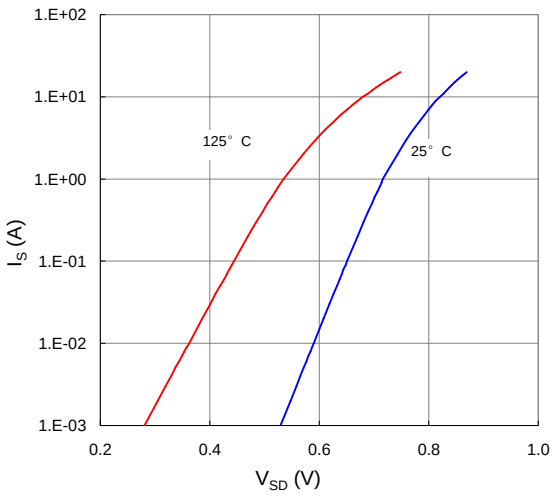


Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

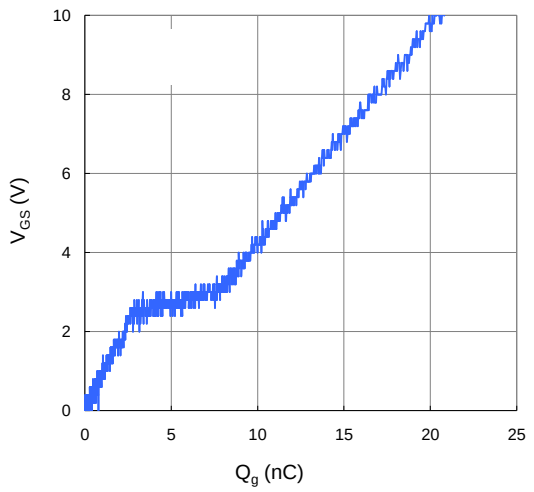


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

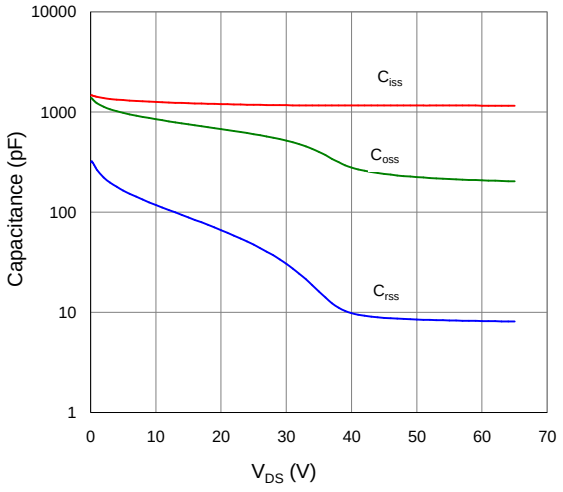


Figure 9. Maximum Safe Operating Area

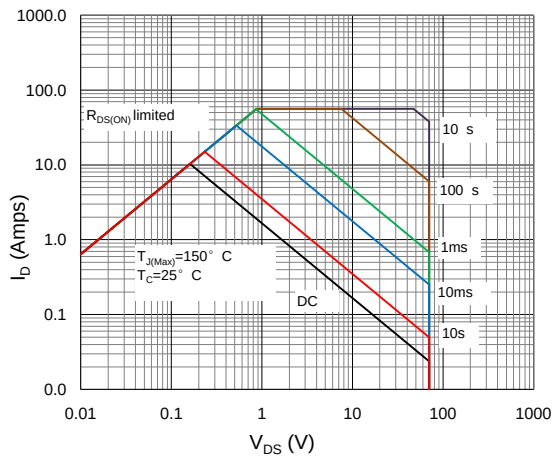


Figure 10. Maximun Drain Current vs. Case Temperature

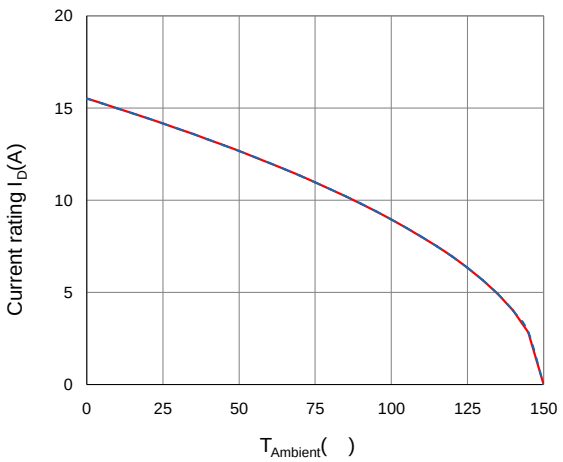
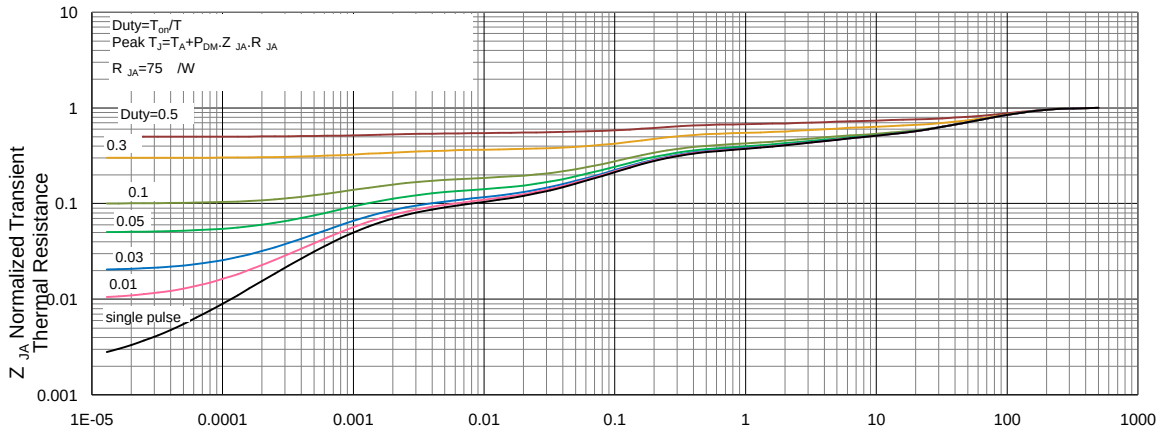


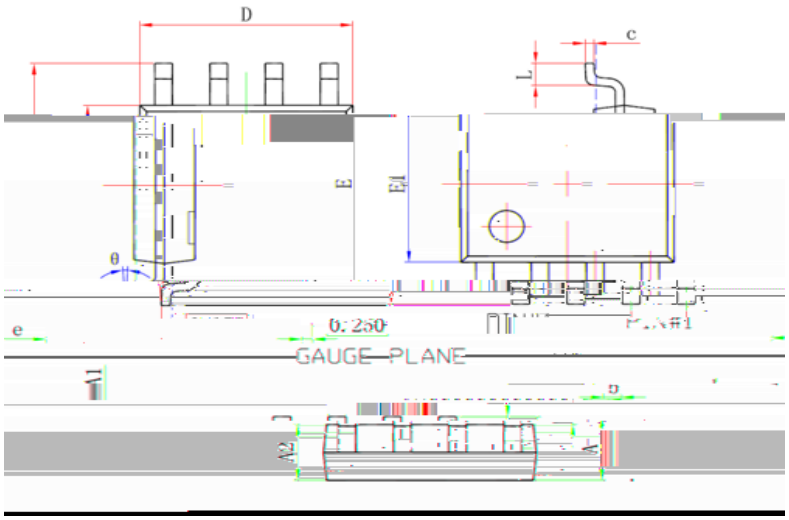
Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient



Inductive switching Test

Package Outline

SOIC-8, 8 leads



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.250	1.650	0.049	0.065
b	0.310	0.510	0.012	0.020
c	0.170	0.250	0.007	0.010
D	4.800	5.000	0.189	0.197
e	1.270 (BSC)		0.050 (SBC)	
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
L	0.400	1.270	0.016	0.031
θ	0°	8°	0°	8°